REMARKS

I. Status of the Claims:

Claims 9-24 are currently pending. Claims 17-24 have been allowed.

By this Amendment, claims 9 and 11-3 have been amended. No new matter has been introduced by this Amendment.

Upon entry of this Amendment, claims 9-24 would be pending.

II. Rejection Under 35 U.S.C. §§102 and 103:

Claims 9-10 and 13-14 have been rejected under 35 U.S.C. §102(e) as being anticipated by Kim (U.S. Patent No. 6,055,272). Claims 11-12 and 15-16 are rejected under 35 U.S.C. §103 as being unpatentable over Jan (U.S. Patent No. 5,363,097). Applicants respectfully disagree with these rejections for the following reasons.

1. U.S. Patent No. 6,055,272 (Kim):

The Examiner alleges that in Kim, the lines inputting the odd and even coefficients into element 10 of Fig. 1 of Kim correspond to a plurality of data buses and element 10 corresponds to a plurality of storages and counters. The Examiner also alleges that there inherently is a selector in Kim.

However, neither the relationship between the odd and even coefficients inputting into run length encoding core 10 and the 2-dimensional symbols, (run 1, level 1) and (run 2, level 2) output from run length encoding core 10, nor the inner configuration and operation of length encoding core 10 is clear. The Examiner alleges that inherently there are a plurality of storages and counters in element 10. However, the passages referred to by the Examiner only indicate

that run length encoding core 10 receives the odd and even coefficients and outputs the 2-dimensional symbols (run 1, level 1) and (run 2, level 2).

Furthermore, Applicants respectfully submit that the run length encoding core 10 of Kim does not include the claimed plurality of data storages storing input data and outputting the same in the order of input. Specifically, the Examiner alleges that inherently there are a plurality of storages storing "level 1" and "level 2" separately in order to have "run 1", "run 2", "level 1" and "level 2" synchronize with the process of zero block detector 30. In such a case, it is necessary to have the output timing of run length encoding core 10 synchronized with the output timing of selection signal mux_sel from zero block detector 30 in order to have MUX1~MUX4 normally operate because zero block detector 30 has counted 32 zeros. That is, the input timing of the odd and even coefficients into run length encoding core 10 need to be synchronized with the output timing of the 2-dimensional symbols (run 1, level 1) and (run 2, level 2) from the run length encoding core 10. In contrast, as seen, for example, in Fig. 14 of the present application, the input timing of the DCT coefficients into the counter (a data counter 13 in the embodiment) is not synchronized with the output timing of the plurality of storages (FIFO 204a, 204b). Accordingly, the plurality of storages in run length encoding core 10 that the Examiner regards to be inherent are different in function and operation from the plurality of the storages of the present invention. That is, the plurality of storages which may inherently exist in run length encoding core 10 are not FIFO which stores input data and outputs the same in the order of input, as claimed in claims 9, 10, 13 and 14. Accordingly, Applicants respectfully submit that claims 9, 10, 13 and 14 are patentably distinguishable from Kim.

2. U.S. Patent No. 5,363,097 (Jan):

The Examiner also alleges that in Jan, Fig. 5 shows a VLD (variable length decoder) 54, a plurality of data buffers 52-1 to 52-6 and a plurality of RLDs (run length decoders) 55-1 to 55-6 that correspond to the decoder, a plurality of data storages, and a generator of claim 12. However, the VLD (variable length decoder) 54 of Fig. 5 of Jan generates a plurality of fix-length data (see column 6, lines 23 to 26). Consequently, the fix length data are provided to each of the plurality of data buffers 52-1 to 52-6 and also the fix-length data are provided to each of the plurality of RLDs 55-1 to 55-6. Therefore, RLDs 55-1 to 55-6 decode the fix-length data respectively and outputs the decoded data corresponding to the fix-length data respectively. In contrast, in the present invention, the generator as claimed in claim 12 refers to generation of DCT coefficients based on data output from the plurality of data storages. Thus, it is respectfully submitted that Jan does not teach or suggest the claimed decoder, plurality of data storages and generator of claim 12. These arguments apply with equal force to the claimed Huffman decoder of claim 11 and methods of claims 15 and 16.

CONCLUSION

Based on the foregoing amendments and remarks, Applicants respectfully request reconsideration and withdrawal of the rejection of claims and allowance of this application.

AUTHORIZATION

The Commissioner is hereby authorized to charge any additional fees which may be required for consideration of this Amendment to Deposit Account No. 13-4500, Order No. 3620-4010.

In the event that an extension of time is required, or which may be required in addition to that requested in a petition for an extension of time, the Commissioner is requested to grant a petition for that extension of time which is required to make this response timely and is hereby authorized to charge any fee for such an extension of time or credit any overpayment for an extension of time to Deposit Account No. 13-4500, Order No. 3620-4010.

Respectfully submitted,
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